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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

&

Office Action Summary	Application No.	Applicant(s)	
	09/834,013	BESMER ET AL.	
	Examiner	**Art Unit**	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _09 August 2004_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-26_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-26_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _12 April 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,313,588 to Nagashige et al. ("Nagashige"), US Patent Number 6,738,821 to Wilson et al. ("Wilson"), and US Patent Number 6,263,445 to Blumenau ("Blumenau").

3. In reference to Claim 1, Nagashige teaches a processor for forming a plurality of commands, which are equivalent to the bus operation information structures, (See Figure 4 and Column 8 Lines 20-23); a command FIFO memory for storing the commands (See Figure 4 and Column 8 Lines 20-23); and a sequencer for processing the commands to perform the bus operations (See Figure 4 and Column 8 Lines 26-28); sequentially forming commands by the processor in the command FIFO memory (See Figure 4 and Column 8 Lines 20-23); storing the commands in the command FIFO memory, which is equivalent to setting control over the bus operation information

structure to the sequencer, since the memory is FIFO (See Figure 4 and Column 8 Lines 20-20); the sequencer inherently checking the command FIFO memory to determine if a first command is present, which is equivalent to determining if the sequencer has control over the first bus operation information structure in the memory; the sequencer processing the first command upon determining that it has control over said first command (See Figure 4 and Column 8 Lines 26-28); the sequencer inherently checking the command FIFO memory to determine if a second command is present, which is equivalent to determining if the sequencer has control over the second bus operation information structure in the memory; the sequencer processing the second command upon determining that it has control over said second command (See Figure 4 and Column 8 Lines 36-40); and the computer system including a bus adapter including the sequencer and the memory spaces (See Figure 4 and Column 7 Lines 51-58). Nagashige does not teach that each bus operation information structure includes both a command and data to be transferred; that the system includes a CPU communicatively coupled to the bus adapter; and that the bus adapter includes the processor. Wilson teaches an encapsulated command, which is equivalent to a bus operation information structure, that includes both commands and data to be transferred (See Figure 4C and Column 14 Lines 38-49). Blumenau teaches a computer system that has a CPU (See Figure 3 and Column 6 Lines 28-33) and a bus adapter that includes a processor and memory (See Figure 3 and Column 6 Lines 46-51 of Blumenau); the CPU sending data to the bus adapter (See Column 6 Lines 36-38 of Blumenau); the processor in the bus adapter receiving data (See Column 6 Lines 36-38

and Column 6 Lines 47-49); and forming packets, which are equivalent to the bus operation information structures (See Figure 8b Numbers 184 and 185, Column 6 Lines 36-38, Column 6 Lines 51-53, and Column 12 Line 66 – Column 13 Line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige with the encapsulated commands containing commands and data of Wilson and the CPU coupled to a bus adapter containing a processor of Blumenau, resulting in the invention of Claim 1, in order to allow the SCSI devices to communicate over an Ethernet network (See Abstract and Column 3 Lines 47-52 of Wilson); to provide a means to connect the host processor to the bus (See Column 6 Lines 35-36 of Blumenau); and to convert the data received from the CPU into a format compatible with the bus (See Column 6 Lines 36-38 of Blumenau).

4. Claims 2, 3, 5, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, and Blumenau as applied to Claim 1 above, and further in view of US Patent Number 6,205,506 to Richardson ("Richardson").

5. In reference to Claim 2, Nagashige, Wilson, and Blumenau teach the limitations as applied to Claim 1 above. Nagashige, Wilson, and Blumenau do not teach a queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure is ready for processing; placing a pointer identifying the first bus operation information structure in

the queue of pointers by the processor upon forming the first bus operation information structure; and reading the pointer identifying the first bus operation information structure from the queue of pointers by the sequencer before processing the first bus operation information structure. Richardson teaches placing pointers to entries in a transaction buffer, which is equivalent to the bus operation information structure, in a queue of pointers by the processor upon creation of said entries, which is also when they are ready for processing (See Column 5 Lines 10-19); and the bus interface unit, which is equivalent to the sequencer, reading the pointer identifying the first entry in the transaction buffer from the queue of pointers before processing the first entry (See Column 5 Lines 19-25). Richardson further teaches the processor connected to the bus interface unit by a cache (See Column 5 Lines 64-67), said cache passing requests to the bus interface unit if it cannot service the request (See Column 1 Lines 22-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, and Blumenau with the pointer queue system of Richardson, resulting in the invention of Claim 2, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

6. In reference to Claim 3, Nagashige, Wilson, Blumenau, and Richardson teach the limitations as applied to Claim 2 above. Nagashige, Wilson, and Blumenau further do not teach setting control over each bus operation information structure to the

sequencer by placing the pointer identifying each bus operation information structure in the queue of pointers. Richardson further teaches that the pointer queues are first-in-first-out (See Column 6 Lines 45-49); that the pointers in the request queue point to entries which are to be transferred from the transaction buffer to the bus (See Column 6 Lines 66-67 and Column 7 Lines 1-10); and that the pointer queues are part of the bus interface unit (See Column 6 Lines 40-45). Therefore, the entries in the requesting queue are inherently controlled by the sequencer upon the pointer to said entry being placed in the request queue.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, and Blumenau with the pointer queue system of Richardson, resulting in the invention of Claim 3, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

7. In reference to Claim 5, Nagashige, Wilson, Blumenau, and Richardson teach the limitations as applied to Claim 2 above. Nagashige, Wilson, and Blumenau further do not teach the queue of pointers being a first queue of pointers and the system further comprising a second queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed; placing a pointer identifying the first bus operation information structure in the second queue of pointers by the sequencer after processing

the first bus operation information structure; reading the pointer identifying the first bus operation information structure from the second queue of pointers by the processor; and forming a third bus operation information structure in the same memory space containing the first bus operation information structure. Richardson further teaches multiple pointer queues (See Column 5 Lines 10-13 and Column 6 Lines 40-51) wherein each pointer is set to identify one of the transaction requests when said request has been processed (See Column 7 Lines 29-31); that a pointer to a transaction that has been completed on the bus can be placed in a completion status queue, which is equivalent to the second queue of pointers (See Column 7 Lines 24-31); transferring the pointer from the completion status queue to the cache which transfers it to the processor (See Column 7 Lines 32-36); and marking the entry in the transaction buffer corresponding to said pointer as empty (See Column 7 Lines 36-39) which allows a new transaction request, which is equivalent to the bus operation information structure, to be loaded into that space in the transaction buffer (See Column 6 Lines 55-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, and Blumenau with the pointer queue system of Richardson, resulting in the invention of Claim 5, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

8. In reference to Claim 6, Nagashige, Wilson, and Blumenau teach the limitations as applied to Claim 1 above. Nagashige, Wilson, and Blumenau do not teach a queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed; placing a pointer identifying the first bus operation information structure in the queue of pointers by the sequencer after processing the first bus operation information structure; reading the pointer identifying the first bus operation information structure from the queue of pointers by the processor; and forming a third bus operation information structure in the same memory space containing the first bus operation information structure. Richardson teaches a queue of pointers wherein each pointer is set to identify one of the transaction requests when said request has been processed (See Column 5 Lines 10-13 and Column 7 Lines 29-31); that a pointer to a transaction that has been completed on the bus can be placed in a completion status queue (See Column 7 Lines 24-31 of Richardson); transferring the pointer from the completion status queue to the cache which transfers it to the processor (See Column 7 Lines 32-36); and marking the entry in the transaction buffer corresponding to said pointer as empty (See Column 7 Lines 36-39) which allows a new transaction request to be loaded into that space in the transaction buffer (See Column 6 Lines 55-58). Richardson further teaches the processor connected to the bus interface unit by a cache (See Column 5 Lines 64-67), said cache passing requests to the bus interface unit if it cannot service the request (See Column 1 Lines 22-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, and Blumenau with the pointer queue system of Richardson, resulting in the invention of Claim 6, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

9. In reference to Claim 7, Nagashige, Wilson, Blumenau, and Richardson teach the limitations as applied to Claim 6 above. Nagashige, Wilson, and Blumenau further do not teach setting control over each bus operation information structure to the processor by placing the pointer identifying each bus operation information structure in the queue of pointers. Richardson teaches that the pointer queues are first-in-first-out (See Column 6 Lines 45-49) and that the pointers in the completion status queue point to entries which are to be transferred from the transaction buffer to the processor (See Column 7 Lines 24-36). Therefore, the entries in the completion status queue are inherently controlled by the processor upon the pointer to said entry being placed in the completion status queue.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, and Blumenau with the pointer queue system of Richardson, resulting in the invention of Claim 7, in order to allow different classes of information to be stored separately as well as to maintain

ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

10. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, Blumenau, and Richardson as applied to Claims 2 and 7 above, and further in view of US Patent Number 6,047,339 to Su et al. ("Su").

11. In reference to Claim 4, Nagashige, Wilson, Blumenau, and Richardson teach the limitations as applied to Claim 2 above. Nagashige, Wilson, Blumenau, and Richardson do not teach the queue of pointers supplying a start flag to the sequencer whenever the queue of pointers contains a pointer that has not been read by the sequencer; asserting the start flag after placing the pointer identifying the first bus operation information structure in the queue of pointers; and determining that the sequencer has control over the first bus operation information structure by receiving the start flag by the sequencer and reading the pointer identifying the first bus operation information structure from the queue of pointers. Su teaches sending a signal to a read controller, which is equivalent to the sequencer, indicating that unread data is present in the memory bank, which is equivalent to the queue of pointers (See Column 4 Lines 37-40 and Column 5 Lines 33-61); asserting the start flag upon placing data in a memory bank (See Column 5 Lines 33-34); and the read controller determining that the data in the memory bank can be read by receiving the start flag and reading the data from the

memory bank, which is equivalent to determining that the sequencer has control over the first bus operation information structure (See Column 5 Lines 46-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, and Richardson with the device of Su, resulting in the invention of Claim 4, in order to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

12. In reference to Claim 8, Nagashige, Wilson, Blumenau, and Richardson teach the limitations as applied to Claim 7 above. Nagashige, Wilson, Blumenau, and Richardson further do not teach the queue of pointers supplying a complete flag to the processor whenever the queue of pointers contains a pointer that has not been read by the processor; asserting the complete flag after placing the pointer identifying the first bus operation information structure in the queue of pointers; and determining that the processor has control over the first bus operation information structure by receiving the complete flag by the processor and reading the pointer identifying the first bus operation information structure from the queue of pointers. Su teaches sending a signal to a read controller, which is equivalent to the processor, indicating that unread data is present in the memory bank, which is equivalent to the queue of pointers (See Column 4 Lines 37-40 and Column 5 Lines 33-61); asserting the start flag, which is equivalent to the complete flag, upon placing data in a memory bank (See Column 5 Lines 33-34); and the read controller determining that the data in the memory bank can be read by

receiving the start flag and reading the data from the memory bank (See Column 5 Lines 46-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, and Richardson with the device of Su, resulting in the invention of Claim 8, in order to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

13. Claims 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, and Blumenau as applied to Claim 1 above, and further in view of US Patent Number 6,434,650 to Morris et al. ("Morris").

14. In reference to Claim 9, Nagashige, Wilson, and Blumenau teach the limitations as applied to Claim 1 above. Nagashige, Wilson, and Blumenau do not teach sending a signal from the processor to the sequencer to start processing the first bus operation information structure upon forming said first bus operation information structure. Morris teaches a transmitter, which is equivalent to the processor, driving a control signal low when it is ready to transmit data to the co-processor, which is equivalent to signaling the sequencer to begin processing (See Figures 1, 1a, and 3, and Column 8 Lines 6-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, and Blumenau with

the signaling system of Morris, resulting in the invention of Claim 9, in order to provide a means of flow control (See Column 6 Lines 63-67 of Morris).

15. In reference to Claim 14, Nagashige, Wilson, Blumenau and Morris teach the limitations as applied to Claim 9 above. Blumenau further teaches the CPU sending data, which is equivalent to I/O messages, to the bus adapter (See Column 6 Lines 36-38); the processor in the bus adapter receiving data (See Column 6 Lines 36-38 and Column 6 Lines 47-49); and forming packets, which are equivalent to the bus operation information structures, compatible with the network protocol from the data received from the CPU (See Column 6 Lines 36-38 and Column 6 Lines 51-53).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, and Blumenau with the signaling system of Morris, resulting in the invention of Claim 14, in order to provide a means of flow control (See Column 6 Lines 63-67 of Morris).

16. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Morris as applied to Claim 9 above, and further in view of US Patent Number 5,726,985 to Daniel et al. ("Daniel").

17. In reference to Claim 10, Nagashige, Wilson, Blumenau and Morris teach the limitations as applied to Claim 9 above. Nagashige, Wilson, Blumenau and Morris do not teach associating the bus operation information structure with a link to the next bus

operation information structure upon forming each bus operation information structure; and after processing each bus operation information structure by the sequencer, determining which bus operation information structure is to be processed next by reading the associated link to the next bus operation information structure. Daniel teaches a FIFO memory in which each element, which is equivalent to the bus operation information structure, contains a link to the next element, said link being maintained by the scheduler, which is equivalent to the processor, said maintenance inherently being performed upon adding an element to the linked-list FIFO (See Column 15 Lines 45-47); and the APU, which is equivalent to the sequencer, determining which element to transmit next based on the link information of the current element, since they are transmitted in FIFO order and each element contains a link to the next element (See Column 29 Lines 35-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau and Morris with the linked FIFO memory of Daniel, resulting in the invention of Claim 10, in order to allow elements to be inserted into the middle of the FIFO structure without disturbing and reordering the remainder of the list (See Column 7 Lines 47-56 of Daniel).

18. In reference to Claim 11, Nagashige, Wilson, Blumenau, Morris, and Daniel teach the limitations as applied to Claim 10 above. Nagashige, Wilson, Blumenau and Morris further do not teach each bus operation information structure including a link field which indicates the next bus operation information structure; and setting the link field of

the bus operation information structure to the next bus operation information structure to associate the bus operation information structure wit the link. Daniel teaches that the link information is contained in a link field of the element (See Figure 7 and Column 15 Lines 40-47); and the link field being maintained by the scheduler, which is equivalent to the processor, said maintenance inherently being performed upon adding an element to the linked-list FIFO (See Column 15 Lines 45-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau and Morris with the linked FIFO memory of Daniel, resulting in the invention of Claim 11, in order to allow elements to be inserted into the middle of the FIFO structure without disturbing and reordering the remainder of the list (See Column 7 Lines 47-56 of Daniel).

19. Claims 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, Blumenau and Morris as applied to Claim 9 above, and further in view of Su.

20. In reference to Claim 12, Nagashige, Wilson, Blumenau and Morris teach the limitations as applied to Claim 9 above. Nagashige, Wilson, Blumenau and Morris do not teach each bus operation information structure including an owner field that indicates whether the processor or the sequencer has control over the bus operation information structure; setting the owner field to the sequencer by the processor to set control over the bus operation information structure to the sequencer upon forming each

bus operation information structure; and setting the owner field to the processor by the sequencer after processing each bus operation information structure. Su teaches a plurality of memory banks, which are equivalent to the bus operation information structures, that each includes a status flag that can be used to indicate ownership of the corresponding bank (See Column 4 Lines 30-32, Column 5 Lines 38-39, and Column 5 Lines 52-54); the write controller, which is equivalent to the processor, setting the status flag to a value of "start", which is equivalent to setting the owner field to the sequencer, upon writing data to the memory bank, which is equivalent to forming a bus operation information structure (See Column 5 Lines 33-34); and the read controller, which is equivalent to the sequencer, setting the status flag to a value of "done", which is equivalent to setting the owner field to the processor, after reading the data in the memory bank (See Column 5 Lines 49-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau and Morris with the device of Su, resulting in the invention of Claim 12, in order to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

21. In reference to Claim 13, Nagashige, Wilson, Blumenau and Morris teach the limitations as in Claim 9 above. Nagashige, Wilson, Blumenau and Morris do not teach setting control over the bus operation information structure to the processor before forming the bus operation information structure; determining whether the sequencer or

the processor has control over the second bus operation information structure after processing the first bus operation information structure; and waiting for the processor to send a signal to the sequencer to start processing the second bus operation information structure upon determining that the processor has control over the second bus operation information structure. Su inherently teaches that each memory bank status flag is initially set to a value of “done”, since a memory location cannot be read from before it is written to; and thereafter, every write operation will be preceded by a read operation, which sets the value of the status flag to “done”, which is equivalent to setting control over the bus operation information structure to the processor before forming each bus operation information structure. Su further teaches the read controller, which is equivalent to the sequencer, determining if the value of the status flag for the second memory bank is “start”, which is equivalent to determining if the processor has control over the second bus operation information structure, after reading the first memory bank, which is equivalent to processing the first bus operation information structure (See Column 5 Lines 49-51 of Su); and waiting until the write controller, which is equivalent to the processor, sets the value of the status flag to “start”, indicating that the read controller now has control of the memory bank (See Column 5 Lines 51-56);

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau and Morris with the device of Su, resulting in the invention of Claim 13, in order to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

22. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, Blumenau, and Su.

23. In reference to Claim 15, Nagashige teaches a bus (See Figure 4 and Column 7 Lines 51-58); a command FIFO memory for storing the commands (analogous to the bus operation information structures) (See Figure 4 and Column 8 Lines 20-23); a sequencer connected to the memory and the bus to perform the bus operations on the bus upon processing the commands (See Figure 4 and Column 7 Lines 51-58); a processor connected to the memory spaces and the sequencer to sequentially form the commands in the memory spaces (See Figure 4 and Column 8 Lines 20-23); the sequencer processing the first command upon determining that it has control over said first command (See Figure 4 and Column 8 Lines 26-28); the sequencer processing the second command upon determining that it has control over said second command (See Figure 4 and Column 8 Lines 36-40); and the computer system including a bus adapter including the sequencer and the memory spaces (See Figure 4 and Column 7 Lines 51-58). Nagashige does not teach that each of said bus operation information structures includes both a command and data to be transferred; a plurality of control indicators indicating control status over the bus operation information structures; said control indicators connected to the sequencer to indicate that the sequencer has control over the bus operation information structure; said control indicators further connected to the processor and generated by the processor causing the sequencer to process the

formed bus operation information structures; the sequencer processing a first one of the bus operation information structures upon receiving a first one of the control indicators and the sequencer processing a second one of the bus operation information structures upon completion of processing the first bus operation information structure if a second one of the control indicators indicates that the sequencer has control over the second bus operation information structure; that the system includes a CPU communicatively coupled to the bus adapter; and that the bus adapter includes the processor. Wilson teaches an encapsulated command, which is equivalent to a bus operation information structure, that includes both commands and data to be transferred (See Figure 4C and Column 14 Lines 38-49). Blumenau teaches a computer system that has a CPU (See Figure 3 and Column 6 Lines 28-33) and a bus adapter that includes a processor and memory (See Figure 3 and Column 6 Lines 46-51); the CPU sending data to the bus adapter (See Column 6 Lines 36-38); the processor in the bus adapter receiving data (See Column 6 Lines 36-38 and Column 6 Lines 47-49); and forming packets, which are equivalent to the bus operation information structures (See Figure 8b Numbers 184 and 185, Column 6 Lines 36-38, Column 6 Lines 51-53, and Column 12 Line 66 – Column 13 Line 3). Su teaches status flags, which are equivalent to the control indicators, for memory banks, which are equivalent to the bus operation information structures (See Column 2 Lines 26-33); a read controller, which is equivalent to the sequencer, connected to the status flags that reads the data in the memory bank, which is equivalent to performing the bus operation described by the bus operation information structure, if the status flag has a value of "start," which is equivalent to indicating the

sequencer has control, (See Column 5 Lines 46-47); a write controller, which is equivalent to the processor, connected to the status flags that sequentially writes data to the memory banks, which is equivalent to forming the bus operation information structures, and sets the status flag to the value of "start" (See Column 5 Lines 33-38); the read controller reading the data in the first memory bank when the first status flag has a value of "start" (See Column 5 Lines 46-47); and the sequencer reading the second memory bank upon completion of reading the first memory bank if the second status flag has a value of "start" (See Column 5 Lines 46-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made would combine the device of Nagashige with the encapsulated commands containing commands and data of Wilson, the CPU coupled to a bus adapter containing a processor of Blumenau, and the device of Su, resulting in the invention of Claim 15, in order to the SCSI devices to communicate over an Ethernet network (See Abstract and Column 3 Lines 47-52 of Wilson); to provide a means to connect the host processor to the bus (See Column 6 Lines 35-36 of Blumenau); and to convert the data received from the CPU into a format compatible with the bus (See Column 6 Lines 36-38 of Blumenau); and to allow the processor to communicate with a sequencer operating at a different speed (See Column 1 Lines 12-28 of Su).

24. Claims 16, 17, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, Blumenau, and Su as applied to Claim 15 above, and further in view of Richardson.

25. In reference to Claim 16, Nagashige, Wilson, Blumenau, and Su teach the limitations as applied to Claim 15 above. Nagashige, Wilson, Blumenau, and Su do not teach the control indicators including a queue of pointers, each pointer being set to identify one of the bus operation information structures when the identified bus operation information structure is ready for processing; the processor sending the pointers to the queue of pointers identifying the formed bus operation information structures in the order that the bus operation information structures were formed after forming the bus operation information structures; the sequencer reading the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers and processes the bus operation information structures in the same order; and the sequencer proceeding to process the second bus operation information structure if the queue of pointers contains a pointer for the second bus operation information structure. Richardson teaches placing pointers to entries in a transaction buffer, which is equivalent to the bus operation information structures, in a queue of pointers by the processor upon creation of said entries, which is also when they are ready for processing (See Column 5 Lines 10-19); placing a pointer to a newly created transaction entry in the queue of pointers upon creation of said entry (See Column 6 Lines 58-61); the bus interface unit, which is equivalent to the sequencer reading a pointer from the head of the FIFO queue of pointers (See Column 7 Lines 6-10); and processing the next transaction entry pointed to by the pointer at the head of the queue of pointers upon completion of processing the first transaction entry (See Column 7

Lines 17-23). Richardson further teaches the processor connected to the bus interface unit by a cache (See Column 5 Lines 64-67), said cache passing requests to the bus interface unit if it cannot service the request (See Column 1 Lines 22-34).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige, Wilson, Blumenau, and Su with the pointer queue system of Richardson, resulting in the invention of Claim 16, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

26. In reference to Claim 17, Nagashige, Wilson, Blumenau, Su, and Richardson teach the limitations as applied to Claim 16 above. Nagashige further teaches setting a command presence indicator, which is equivalent to the start flag, that indicates the presence of a command in the command queue that hasn't been processed by the sequencer (See Abstract and Column 8 Lines 23-26); and the sequencer processing the next command in the command queue upon completing processing the previous command if the command presence indicator is set and upon the command presence indicator being set if no command is currently being processed by the sequencer (See Abstract and Column 8 Lines 26-42).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige, Wilson, Blumenau, and Su with the pointer queue system of Richardson, resulting in the inventions of Claim 17, in order to allow different classes of

information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

27. In reference to Claim 18, Nagashige, Wilson, Blumenau, and Su teach the limits as applied to Claim 15 above. Su further teaches the write controller writing data to the memory, which is equivalent to forming the second bus operation information structure of Claim 18 upon completion of writing the first memory bank if there is a memory bank available (See Column 5 Lines 33-45). Nagashige, Wilson, Blumenau, and Su do not teach the control indicators including a queue of pointers wherein each pointer is set to identify one of the bus operation information structures when the identified bus operation information structure has been processed by the sequencer and the memory space containing the processed bus operation information structure is available for a new bus operation information structure to be formed therein; the sequencer sending the pointers to the queue of pointers identifying the available memory spaces in the order that the bus operation information structures contained therein were processed after processing the bus operation information structures; the processor reading the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers and forming the next bus operation information structure in one of the available memory spaces; and the processor proceeding to form the second bus operation information structure if there is at least the one available memory space upon completing forming the first bus operation information structure. Richardson teaches a

queue of pointers wherein each pointer identifies a transaction that has completed processing and the buffer space of said transaction is available (See Column 7 Lines 30-40); the queue of pointers from the sequencer identifying the available memory spaces being a FIFO queue, which is equivalent to sending the pointers to the queue of pointers in the order that they were processed (See Column 6 Lines 40-52); a pointer being acted on when it reaches the head of a FIFO queue, which is equivalent to the processor reading the pointers from the queue of pointers in the order in which the pointers were sent to the queue of pointers (See Column 7 Lines 33-37).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige, Wilson, Blumenau, and Su with the pointer queue system of Richardson, resulting in the invention of Claim 18, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

28. In reference to Claim 19, Nagashige, Wilson, Blumenau, Su, and Richardson teach the limitations as applied to Claim 18 above. Su further teaches sending a signal to a write controller, which is equivalent to the processor, indicating that there is a location in the memory bank, which is equivalent to the queue of pointers, that has not been acted on by the write controller (See Column 4 Lines 37-40 and Column 5 Lines 33-61); and writing data to the next memory bank, which is equivalent to forming the next bus operation information structure, upon completing writing data to the previous

memory bank if there is an available memory bank and upon receiving the done flag, which is equivalent to the complete flag, if none of the memory banks are currently available (See Column 5 Lines 33-42).

One of ordinary skill in the art at the time the invention was made would combine the device of Nagashige, Wilson, Blumenau, and Su with the pointer queue system of Richardson, resulting in the invention of Claim 19, in order to allow different classes of information to be stored separately as well as to maintain ordering information for each entry in the transaction buffer (See Abstract, Column 5 Lines 19-22, Column 6 Lines 40-45, and Column 8 Lines 15-18 of Richardson).

29. Claims 20, 21, 22, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, Blumenau, and Su as applied to Claim 15 above, and further in view of US Patent Number 6,052,133 to Kang ("Kang").

30. In reference to Claim 20, Nagashige, Wilson, Blumenau, and Su teach the limitations as applied to Claim 15 above. Su further teaches that the status flags can be stored in the memory device, which is equivalent to each bus operation information structure including the control information indicating control status, (See Column 4 Lines 30-32). Nagashige, Wilson, Blumenau, and Su do not teach the sequencer performing the bus operation described by each bus operation information structure if the sequencer receives a start signal; the processor sending the start signal to the sequencer to start processing the first bus operation information structure; and the

sequencer processing the first bus operation information structure upon receiving the start signal. Kang teaches a PCI bridge/cache controller unit, which is equivalent to the processor, that sends a start signal to a unified graphics/video controller, which is equivalent to the sequencer, followed by a command and corresponding address and data information, which is equivalent to the bus operation information structure (See Figure 6, Column 6 Lines 66-67, and Column 7 Lines 1-19).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, and Su with the device of Kang, resulting in the invention of Claim 20, in order to produce a more efficient device, since the sequencer will only receive commands from one place (See Column 2 Lines 37-41 of Kang).

31. In reference to Claim 21, Nagashige, Wilson, Blumenau, Su, and Kang teach the limitations as applied to Claim 20 above. Blumenau further teaches the CPU sending data, which is equivalent to I/O messages, to the bus adapter (See Column 6 Lines 36-38); the processor in the bus adapter receiving data (See Column 6 Lines 36-38 and Column 6 Lines 47-49); and forming packets, which are equivalent to the bus operation information structures, compatible with the network protocol from the data received from the CPU (See Column 6 Lines 36-38 and Column 6 Lines 51-53); and the data defining the I/O operations to be performed through the bus (See Column 6 Lines 36-38). The CPU of Blumenau would inherently be responsive to software programming to prepare the data and to send the data to the bus adapter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, and Su with the device of Kang, resulting in the invention of Claim 21, in order to produce a more efficient device, since the sequencer will only receive commands from one place (See Column 2 Lines 37-41 of Kang).

32. In reference to Claim 22, Nagashige, Wilson, Blumenau, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches the write controller setting the status flag for a memory bank to a value of "start", which is equivalent to indicating that the sequencer has control over the bus operation information structure, upon writing data to the memory bank (See Column 5 Lines 33-34); and the read controller setting the status flag for a memory bank to a value of "done", which is equivalent to indicating that the processor has control over the bus operation information structure, upon reading the data in the memory bank (See Column 5 Lines 47-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, and Su with the device of Kang, resulting in the invention of Claim 22, in order to produce a more efficient device, since the sequencer will only receive commands from one place (See Column 2 Lines 37-41 of Kang).

33. In reference to Claim 23, Nagashige, Wilson, Blumenau, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches that the read controller

does not read the data from a memory bank if the status flag does not have a value of "start", which is equivalent to indicating that the sequencer has control over the bus operation information structure (See Column 5 Lines 49-56). Nagashige, Wilson, Blumenau, and Su further do not teach the sequencer waiting to receive the start signal from the processor before processing the second bus operation information structure. Kang further teaches that the graphics/video controller waits to receive the start signal before beginning to perform the task specified by the command (See Column 7 Lines 5-14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, and Su with the device of Kang, resulting in the invention of Claim 23, in order to produce a more efficient device, since the sequencer will only receive commands from one place (See Column 2 Lines 37-41 of Kang).

34. In reference to Claim 24, Nagashige, Wilson, Blumenau, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches that each memory bank can include a status flag that also indicates ownership (See Column 4 Lines 30-32, Column 5 Lines 38-39, and Column 5 Lines 52-54); and the status flag being set by the write controller, which is equivalent to the processor, after writing data to the memory bank, which is equivalent to forming the bus operation information structure, to indicate that the data has been written and may be read by the read controller, which is equivalent to the sequencer of Claim 24.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, and Su with the device of Kang, resulting in the invention of Claim 24, in order to produce a more efficient device, since the sequencer will only receive commands from one place (See Column 2 Lines 37-41 of Kang).

35. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashige, Wilson, Blumenau, Su, and Kang as applied to Claim 20 above, and further in view of Daniel.

36. In reference to Claim 25, Nagashige, Wilson, Blumenau, Su, and Kang teach the limitations as applied to Claim 20 above. Su further teaches the read controller, which is equivalent to the sequencer, checking the status flag, which is equivalent to the control information, to determine if it should begin reading the data in the memory bank, which is equivalent to the bus operation information structure, (See Column 5 Lines 49-56). Nagashige, Wilson, Blumenau, Su, and Kang do not teach each bus operation information structure including link information indicating a next one of the bus operation information structures to be processed by the sequencer after processing a current one of the bus operation information structures to be processed by the sequencer after processing a current one of the bus operation information structures; and the sequencer determining which one of the bus operation information structures is the next bus operation information structure from the link information of the current bus operation

information structure and determining whether to begin processing the next bus operation information structure from the control information of the next bus operation information structure. Daniel teaches a FIFO memory in which each element, which is equivalent to the bus operation information structure, contains a link to the next element to be transmitted, which is equivalent to being processed by the sequencer, after transmitting the current element (See Figures 3 and 4, Column 7 Lines 44-46, and Column 29 Lines 24-39); and the APU, which is equivalent to the sequencer, determining which element to transmit next based on the link information of the current element, since they are transmitted in FIFO order and each element contains a link to the next element (See Column 29 Lines 35-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, Su, and Kang with the linked FIFO memory of Daniel, resulting in the invention of Claims 25, in order to allow elements to be inserted into the middle of the FIFO structure without disturbing and reordering the remainder of the list (See Column 7 Lines 47-56 of Daniel).

37. In reference to Claim 26, Nagashige, Wilson, Blumenau, Su, Kang, and Daniel teach the limitations as applied to Claim 25 above. Nagashige, Wilson, Blumenau, Su, and Kang further do not teach each bus operation information structure including a link field containing the link information; and the link field of each bus operation information structure being set by the processor to indicate the next bus operation information

structure upon forming the current bus operation information structure. Daniel further teaches that the link information is contained in a link field of the element (See Figure 7 and Column 15 Lines 40-47); and the link field being maintained by the scheduler, which is equivalent to the processor of, said maintenance inherently being performed upon adding an element to the linked-list FIFO (See Column 15 Lines 45-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nagashige, Wilson, Blumenau, Su, and Kang with the linked FIFO memory of Daniel, resulting in the invention of Claims 26, in order to allow elements to be inserted into the middle of the FIFO structure without disturbing and reordering the remainder of the list (See Column 7 Lines 47-56 of Daniel).

Response to Arguments

38. Applicant's arguments filed 9 August 2004 have been fully considered but they are not persuasive.

39. Applicant has argued that the prior art does not teach "a processor for forming a plurality of bus operation information structures, ... said each bus operation information structure including both a command and data" and "the computer system includes a central processing unit (CPU) and a bus adapter, the bus adapter including the processor, the sequencer and the memory spaces, the CPU being communicatively

coupled to the bus adapter." The Examiner notes that, as shown in the above rejections, Nagashige teaches a processor for forming a plurality of bus operation information structures (See Figure 4 and Column 8 Lines 20-23) and the bus adapter including the sequencer and the memory spaces (See Figure 4 and Column 7 Lines 51-58 of Nagashige). Wilson teaches that the bus operation information structure includes both a command and data (See Figure 4C and Column 14 Lines 38-49). Blumenau teaches a computer system that has a CPU (See Figure 3 and Column 6 Lines 28-33) and a bus adapter that includes a processor and memory (See Figure 3 and Column 6 Lines 46-51 of Blumenau); the CPU sending data to the bus adapter (See Column 6 Lines 36-38 of Blumenau); the processor in the bus adapter receiving data (See Column 6 Lines 36-38 and Column 6 Lines 47-49); and forming the bus operation information structures (See Figure 8b Numbers 184 and 185, Column 6 Lines 36-38, Column 6 Lines 51-53, and Column 12 Line 66 – Column 13 Line 3). The Examiner further notes that in the above rejections, the CPU (See Figure 4) of Nagashige is being equated to the processor of the claims, the CPU (See Figure 3 Number 40) of Blumenau is being equated to the CPU communicatively coupled to the bus adapter, and the processor (See Figure 3 Number 41) of Blumenau is being equated to the processor of the claims included in the bus adapter. The Examiner further notes that the processor (See Figure 3 Number 41) of Blumenau forms a control data block (See Figure 8b Number 185 and Column 12 Line 66 – Column 13 Line 3) which is being equated to the bus operation information structure of the claims.

40. In response to Applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

41. In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner notes that, as shown in the above rejections, motivation for the combination of the features of the references relied upon in the rejections are found in the references.

42. In response to Applicant's argument that the Examiner has combined an excessive number of references, reliance on a large number of references in a rejection

does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

Conclusion

43. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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